

Performance of Linear Block Codes Concatenated with Differential PSK

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Abstract—In this letter we investigate the bit and frame error rate performance of various linear block codes when concatenated with a differential phase shift keying modulator. The codes considered include single parity check, Hamming and product codes. We find block codes which significantly improve the frame error rate performance over previous results. An EXIT chart analysis is included.

Index Terms—Accumulator, Hamming code, product code.

I. INTRODUCTION

THE serial concatenation of a linear block code with a rate-1 recursive convolutional code (or accumulator) has been shown to provide good performance in *additive white Gaussian noise* (AWGN) channels [3]. Much attention has been focused on the choice of linear block code. Proposed codes include repetition [3], concatenated *single parity check* (SPC) [9], Hamming [6], [4] and *extended Bose Chaudhuri Hocquenghem* (eBCH) [8] codes. More recently, researchers have looked at replacing the accumulator with a (rate-1) *M*-ary differential phase shift keying (*M*-DPSK) modulator [5], [10], which allows reasonable performance for an unknown phase. SPC codes [5] and *double parity check* (DPC) codes [10] have been proposed for use with the DPSK modulator. They allow good *bit error rate* (BER) performance to be achieved in the waterfall region and have error floors below 10^{-6} . However, we have found the *frame error rate* (FER) performance starts to floor below 10^{-3} .

In this letter we investigate the BER and FER performance of various linear block codes concatenated with a DPSK modulator. Our aim is to significantly improve the FER performance compared to [5], [10]. The cost of the lower error floor is a slight loss in BER and/ or FER performance in the waterfall region or a loss in code rate.

II. SYSTEM DESCRIPTION

The system under consideration consists of an encoder for a (n, k, d_{min}) linear block code serially concatenated with a *M*-DPSK encoder (with $M = 8$), where n is the code length, k is the number of data bits and d_{min} is the minimum Hamming distance. A bit interleaver of length N , denoted π , separates the two encoders as shown in Fig. 1(a). The N bits from the interleaver result in N/m *M*-DPSK symbols, where $m = \log_2(M)$. Note that N is chosen such that $N = \alpha m$ and $N = \beta n$, where α and β are integers. The sequence of N/m *M*-DPSK symbols defines a frame.

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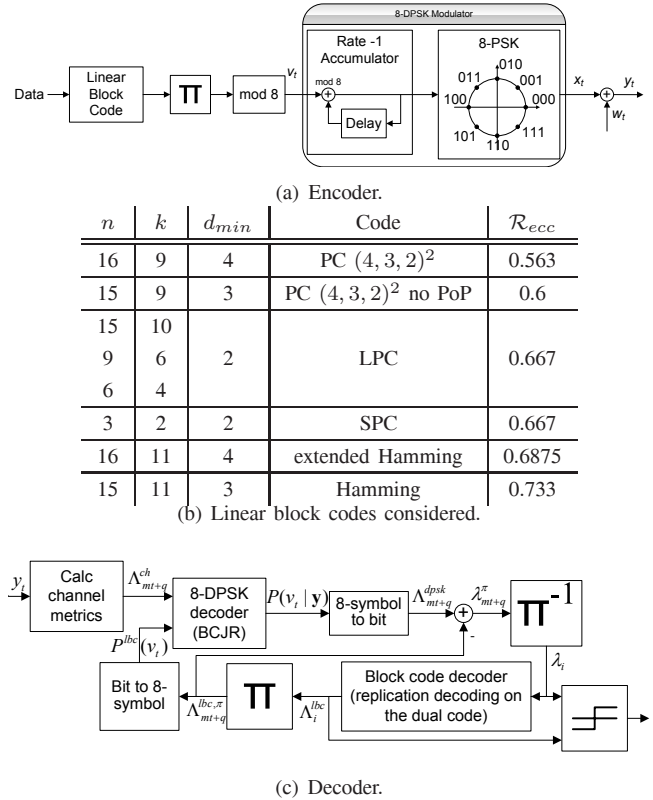


Fig. 1. Encoder, component codes and decoder.

An AWGN channel is considered. The received signal is given by $y_t = x_t + w_t$, where x_t is the t^{th} transmitted *M*-DPSK symbol and w_t is the t^{th} complex AWGN sample with variance $N_0/2 = (2m\mathcal{R}_{ecc}10^{SNR/10})^{-1}$ in each dimension, where \mathcal{R}_{ecc} is the code rate of the block code and SNR is the signal to noise ratio in *Decibels* (dB). Results in [5] show only a slight loss in performance when there is an unknown phase. Therefore, as in [10] we do not simulate an unknown phase.

A. Linear Block Codes

We now discuss the linear block codes considered (summarized in Fig. 1(b)). We are primarily interested in rate $\mathcal{R}_{ecc} = 2/3$ codes. The code is denoted C and a codeword is denoted $c = [u_1, \dots, u_k, p_1, \dots, p_{n-k}]$, where u_i is the i^{th} data bit and p_i is the i^{th} parity bit. For comparison purposes we consider the $(3, 2, 2)$ SPC code discussed in [5]. In [10] two types of DPC codes were proposed. Only the DPC-I codes offer rates greater than $\mathcal{R}_{ecc} = 1/2$. The $(3, 2, 2)$ SPC code is the highest rate DPC-I code with $\mathcal{R}_{ecc} = 2/3$. The parity bits are defined by $p_i = u_i \oplus u_{i+1}$ for $1 \leq i \leq k-1$. The EXIT chart [11] for the $(3, 2, 2)$ SPC code is shown in Fig. 2.

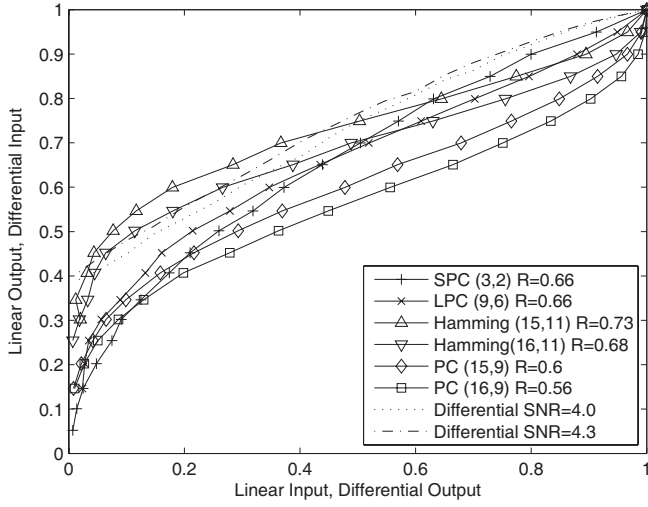


Fig. 2. EXIT charts for various linear block codes.

It has a bottleneck at high mutual information impairing final convergence, which is expected to adversely impact the high SNR FER.

We developed the following $\mathcal{R}_{ecc} = 2/3$, $d_{min} = 2$ linked parity check (LPC) codes by linking several (3, 2, 2) SPC codes together. This is done by adding ones in the positions immediately above and below each pair of ones in the parity check section of the generator matrix. Linking three codes results in a (9, 6, 2) LPC code with generator matrix

$$\mathbf{G} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 & 1 \end{bmatrix}. \quad (1)$$

The parity bits are defined by $p_i = u_{2i-2} \oplus u_{2i-1} \oplus u_{2i} \oplus u_{2i+1}$ for $i = 1, \dots, k/2$ (k must be even), where $u_{k+1} = u_1$ and $u_0 = u_k$. These codes move the bottleneck in Fig. 2 to lower mutual information, which should improve final convergence at the cost of waterfall region performance.

The M -DPSK modulator was also concatenated with a $(4, 3, 2)^2 = (16, 9, 4)$ product code (PC) and a (15, 9, 3) PC without the parity-on-parity (PoP) bit. In addition, the (15, 11, 3) Hamming code and the (16, 11, 4) extended Hamming code were considered. These component codes have higher values of d_{min} , which should result in lower error floors. Fig. 2 shows the higher rate Hamming codes require larger SNR to converge due to a bottleneck at low mutual information. The PCs give excellent performance for the entire decoding process, but have the lowest rates.

A mix of codewords from different codes can be used [7] to modify the code rate and performance. For example, by creating $N/2$ bits using the (15, 9, 3) PC and $N/2$ bits using the (15, 11, 3) Hamming code the overall rate is $\mathcal{R}_{ecc} = 2/3$.

The M -DPSK encoder uses natural mapping [5] of bits to symbols for the Hamming and PCs. The alternate mapping proposed in [5], [10] was used for the SPC and LPC codes.

B. Decoder

The concatenated system is decoded using iterative decoding as shown in Fig. 1(c). The differential (DPSK) code is decoded using the BCJR algorithm [1] and the linear block code is decoded using replication decoding [2]. The input and output metrics for these algorithms are briefly described below. See [5], [1], [2] for more details.

The channel *log likelihood ratio* (LLR) for the $(mt + q)^{th}$ transmitted bit is given by [5], [10]

$$\Lambda_{mt+q}^{ch} = \log \frac{P(y_t | g_{mt+q} = 0)}{P(y_t | g_{mt+q} = 1)} = \log \frac{\sum_{\hat{x}_t | g_{mt+q}=0} P(y_t | \hat{x}_t)}{\sum_{\hat{x}_t | g_{mt+q}=1} P(y_t | \hat{x}_t)}, \quad (2)$$

where $q = 0, 1, \dots, m-1$, g_{mt+q} is the q^{th} bit labelling the hypothesized constellation point at symbol time t , \hat{x}_t , and

$$p(y_t | \hat{x}_t) \propto e^{-|y_t - \hat{x}_t|^2 / N_0}. \quad (3)$$

The inputs to the M -DPSK BCJR decoder are the channel symbol probability densities of (3) and the extrinsic symbol probabilities from the linear block code's decoder for the t^{th} symbol, $P^{lbc}(v_t)$. Initially, $P^{lbc}(v_t) = 1/M$ is used for all M possible symbols.

The M -DPSK symbol probabilities from the BCJR decoder, $P(v_t | \mathbf{y})$, are converted to LLR bit probabilities using

$$\Lambda_{mt+q}^{dpsk} = \log \frac{P(v_t | g_{mt+q} = 0)}{P(v_t | g_{mt+q} = 1)} = \log \frac{\sum_{\hat{v}_t | g_{mt+q}=0} P(\hat{v}_t | \mathbf{y})}{\sum_{\hat{v}_t | g_{mt+q}=1} P(\hat{v}_t | \mathbf{y})}, \quad (4)$$

where $q = 0, 1, \dots, m-1$ and \mathbf{y} is the received signal vector. The extrinsic bit information from the BCJR decoder is

$$\lambda_{mt+q}^{\pi} = \Lambda_{mt+q}^{dpsk} - \Lambda_{mt+q}^{lbc, \pi}, \quad (5)$$

where $\Lambda_{mt+q}^{lbc, \pi}$ is the interleaved extrinsic bit LLR from the block code's decoder. Deinterleaving λ_{mt+q}^{π} gives λ_i .

Replication decoding [2] is used to decode the linear block code, \mathbf{C} . The resulting (uninterleaved) extrinsic LLR for the i^{th} bit is given by $\Lambda_i^{lbc} =$

$$\log \left(\frac{1 + \sum_{\mathbf{c}' \in \{\mathbf{c}'\}_{i0}} \prod_{\substack{j \in J_{\mathbf{c}'}, \\ i \neq j}} \tanh\left(\frac{\lambda_j}{2}\right) + \sum_{\mathbf{c}' \in \{\mathbf{c}'\}_{i1}} \prod_{\substack{j \in J_{\mathbf{c}'}, \\ i \neq j}} \tanh\left(\frac{\lambda_j}{2}\right)}{1 + \sum_{\mathbf{c}' \in \{\mathbf{c}'\}_{i0}} \prod_{\substack{j \in J_{\mathbf{c}'}, \\ i \neq j}} \tanh\left(\frac{\lambda_j}{2}\right) - \sum_{\mathbf{c}' \in \{\mathbf{c}'\}_{i1}} \prod_{\substack{j \in J_{\mathbf{c}'}, \\ i \neq j}} \tanh\left(\frac{\lambda_j}{2}\right)} \right), \quad (6)$$

where \mathbf{c}' is a word in the dual code \mathbf{C}' , $J_{\mathbf{c}'}$ is the set of indices $j = 0, 1, \dots, n-1$ corresponding to the positions of 1's in \mathbf{c}' , and $\{\mathbf{c}'\}_{i0}$ and $\{\mathbf{c}'\}_{i1}$ are the sets of codewords having 0 and 1 in their i^{th} positions, respectively.

The probabilities for the $(mt + q)^{th}$ bit, c_{mt+q} , after decoding the block code are calculated using

$$P(c_{mt+q} = 0) = \frac{\Lambda_{mt+q}^{lbc, \pi}}{1 + \Lambda_{mt+q}^{lbc, \pi}}, \quad P(c_{mt+q} = 1) = \frac{1}{1 + \Lambda_{mt+q}^{lbc, \pi}}. \quad (7)$$

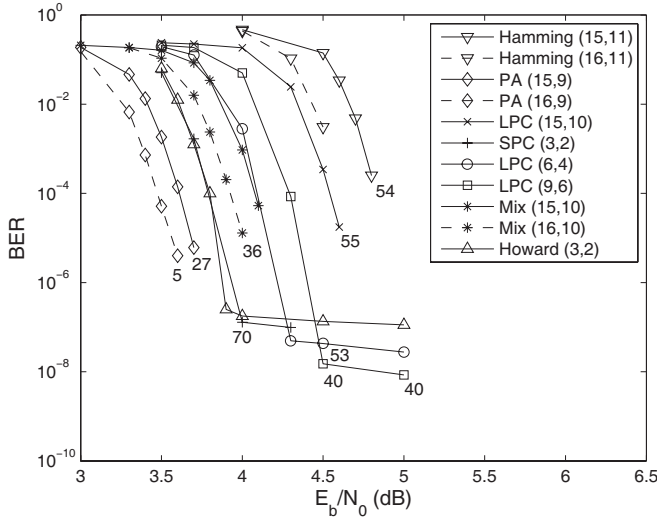


Fig. 3. BER performance for various linear block codes.

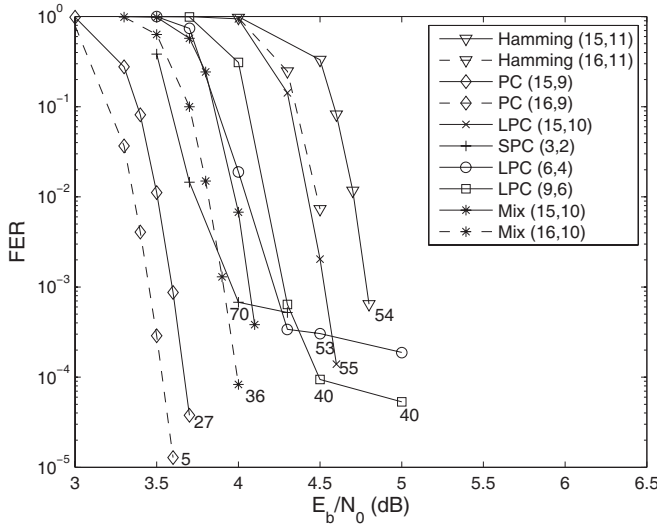


Fig. 4. FER performance for various linear block codes.

The associated symbol probabilities are calculated using

$$P^{lbc}(v_t = X^d) = \prod_{q=1}^m P(c_{mt+q} = C_q^d), \quad (8)$$

where $d = 0, \dots, M-1$, X^d is the d^{th} symbol in the constellation, labelled by bits (C_1^d, \dots, C_m^d) . These probabilities are used to calculate the soft input to the M -DPSK BCJR decoder. Decoding continues until convergence or a maximum number of iterations is reached. The final decision for the i^{th} bit is the hard decision on $\Lambda_i^{lbc} + \lambda_i$.

III. SIMULATION RESULTS

Fig. 3 and Fig. 4 show the BER and FER performance¹ of the concatenated codes, respectively, where E_b is the data bit energy. We used an S -random bit interleaver with $S = 9$ and $N \approx 15000$ bits². The (3, 2) SPC code results of Howard et.

al. [5] vary slightly from our own. This is most likely due to the use of a different interleaver. The LPC codes can lower the error floor compared to the SPC code at the cost of waterfall performance.

As can be seen the PCs offer the best performance, showing no error floor at a FER of 10^{-4} . This is at the cost of code rate. Due to a larger d_{min} , the Hamming codes are also expected to have a low FER error floor [6]. Due in part to their higher rate, they require higher SNR to decode.

Fig. 3 and Fig. 4 show mixed codes, where an equal number of PC and (extended) Hamming codewords are used giving overall rate $\mathcal{R}_{ecc} = 0.625$ for $n = 16$ and $\mathcal{R}_{ecc} = 2/3$ for $n = 15$. This provides a good compromise between waterfall performance, error floor performance and rate.

IV. CONCLUSIONS

We investigated the use of various linear block codes concatenated with an 8-DPSK modulator. We have significantly reduced the FER error floor. In particular, the PCs resulted in a significantly lower error floor at the cost of rate and decoding complexity. The codes presented allow tradeoffs between code rate, decoding complexity, waterfall (low SNR) and error floor (high SNR) performance. Using a mixture of (extended) Hamming codes and PCs provided a good compromise between these factors.

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¹The number of frame errors is stated if less than 100.

²For $n = 3, 6, 15$ we use $N = 15000$, for $n = 9$ we use $N = 15003$ and for $n = 16$ we use $N = 15024$ except for the mixed (16, 11)/(16, 9) code which uses $N = 14976$.